SCLS160B - DECEMBER 1982 - REVISED MAY 1997

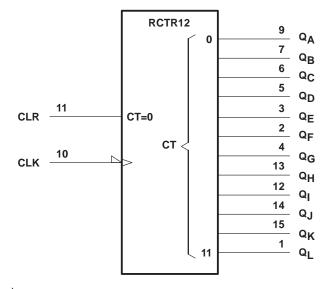
 Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

description

The 'HC4040 are 12-stage asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

The SN54HC4040 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC4040 is characterized for operation from –40°C to 85°C.

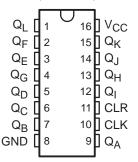
logic symbol†



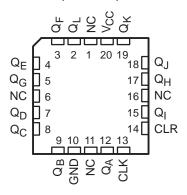
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, DB, J, N, PW, and W packages.

SN54HC4040 . . . J OR W PACKAGE SN74HC4040 . . . D, DB, N, OR PW PACKAGE (TOP VIEW)



SN54HC4040 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

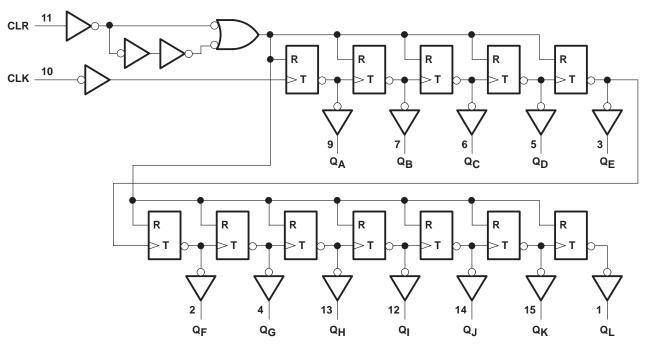


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logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, PW, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V _{CC}		_0.5 \/ to 7 \/
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see	ee Note 1)	±20 mA
Output clamp current, IOK (VO < 0 or VO > VCO	C) (see Note 1)	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$		±25 mA
Continuous current through V _{CC} or GND		±50 mA
Package thermal impedance, θ _{JA} (see Note 2)	: D package	113°C/W
	DB package	131°C/W
	N package	78°C/W
	PW package	149°C/W
Storage temperature range, T _{stq}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.



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recommended operating conditions

			SN	SN54HC4040		SN	74HC40	40	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNII
VCC	Supply voltage		2	5	6	2	5	6	V
VIH High-level input voltage	V _{CC} = 2 V	1.5			1.5				
	V _{CC} = 4.5 V	3.15			3.15			V	
		V _{CC} = 6 V	4.2			4.2			
		V _{CC} = 2 V	0		0.5	0		0.5	
VIL		V _{CC} = 4.5 V	0		1.35	0		1.35	V
		V _{CC} = 6 V	0		1.8	0		1.8	
VI	Input voltage		0		VCC	0		VCC	V
٧o	Output voltage		0		VCC	0		VCC	V
	Input transition (rise and fall) time	V _{CC} = 2 V	0		1000	0		1000	
t _t †		$V_{CC} = 4.5 \text{ V}$	0		500	0		500	ns
		V _{CC} = 6 V	0		400	0		400	
TA	Operating free-air temperature		-55		125	-40		85	°C

[†] If this device is used in the threshold region (from V_{IL}max = 0.5 V to V_{IH}min = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t_t = 1000 ns and V_{CC} = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS		Vaa	T _A = 25°C			SN54HC4040		SN74HC4040		LINIT	
PARAMETER	lESI CC	TEST CONDITIONS V _{CC}		MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT	
VOH VI = VIH or VIL			2 V	1.9	1.998		1.9		1.9			
	I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4				
	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V	
		$I_{OH} = -4 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		1	
		$I_{OH} = -5.2 \text{ mA}$	6 V	5.48	5.8		5.2		5.34			
	VI = VIH or VIL	I _{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1		
			4.5 V		0.001	0.1		0.1		0.1		
VOL			6 V		0.001	0.1		0.1		0.1	V	
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33]	
				$I_{OL} = 5.2 \text{ mA}$	6 V		0.15	0.26		0.4		0.33
lį	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA	
Icc	$V_I = V_{CC}$ or 0,	IO = 0	6 V			8		160		80	μΑ	
Ci			2 V to 6 V		3	10		10		10	pF	

SN54HC4040, SN74HC4040 12-BIT ASYNCHRONOUS BINARY COUNTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	T _A = :	25°C	SN54H	C4040	SN74H	C4040	UNIT		
			VCC	MIN	MAX	MIN	MAX	MIN	MAX	UNIT		
f _{clock} Clock frequency			2 V	0	5.5	0	3.7	0	4.3			
		4.5 V	0	28	0	19	0	22	MHz			
		6 V	0	33	0	22	0	25				
A Dulca divertica		2 V	90		135		115					
		CLK high or low	4.5 V	18		27		23				
	Pulse duration			6 V	15		23		20		ns	
t _W	ruise duration	CLR high	2 V	70		105		90		115		
			4.5 V	14		21		18				
			6 V	12		18		15				
					2 V	60		90		75		
t _{su}	Setup time, CLR inactive before CLK	\downarrow	4.5 V	12		18		15		ns		
			6 V	10		15		13				

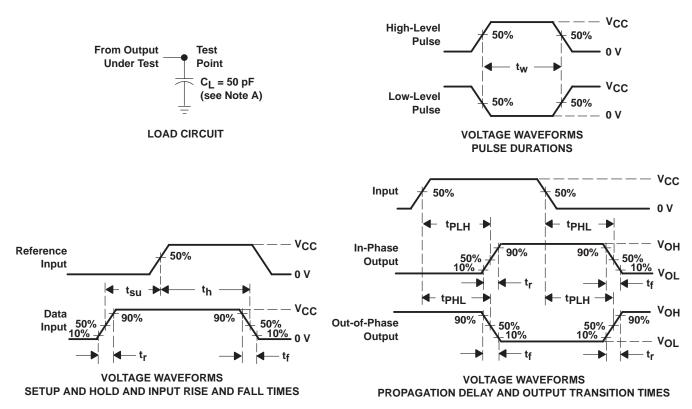
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	Vaa	T,	√ = 25°C	;	SN54H	C4040	SN74H	C4040	UNIT
PARAMETER	(INPUT)		VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	5.5	10		3.7		4.3		
fmax			4.5 V	28	45		19		22		MHz
			6 V	33	53		22		25		
^t pd			2 V		62	150		225		190	
	CLK	Q _A	4.5 V		16	30		45		38	⊣ ∣
			6 V		12	26		38		32	
			2 V		63	140		210		175	
^t PHL	CLR	Any	4.5 V		17	28		42		35	ns
			6 V		13	24		36		30	
		Any	2 V		28	75		110		95	
t _t			4.5 V		8	15		22		19	ns
			6 V		6	13		19		16	

operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load	88	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.

- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \ \Omega$, $t_f = 6 \ ns$, $t_f = 6 \ ns$.
- C. For clock inputs, $f_{\mbox{max}}$ is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

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